I CLAIM:

1. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

a switch coupled between a voltage source and a source terminal of said PMOS transistor, said switch operative to raise said source terminal to a voltage greater than ground potential in response to a transition from DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor.

2. The electrical circuit of claim 1 wherein said PMOS transistor comprises a low threshold voltage (V_{tp}) PMOS transistor.

3. The electrical circuit of claim 1 wherein said switch comprises at least one transistor operative to raise said source terminal to said voltage greater than said ground potential in response to receiving a voltage transition on a control line indicating the end of DRAM standby mode.

4. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-

coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

at least one transistor operative to maintain a source terminal of said PMOS transistor at about ground potential during DRAM standby mode; and

a switch coupled between a voltage source and said source terminal, said switch operative to raise said source terminal to a voltage greater than said ground potential in response to a transition from said DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor.

5. The electrical circuit of claim 4 wherein said PMOS transistor comprises a low threshold voltage (V_{tp}) PMOS transistor.

6. The electrical circuit of claim 5 wherein said V_{tp} is slightly greater than said differential voltage.

7. The electrical circuit of claim 6 wherein said differential voltage between said gate terminal and said drain terminal causes said low V_{tp} PMOS transistor to turn "sub-threshold ON."

8. The electrical circuit of claim 4 wherein said at least one transistor maintains said

source terminal at about ground potential in response to receiving a voltage transition on a control line indicating DRAM standby mode.

9. The electrical circuit of claim 4 wherein said at least one transistor comprises two transistors operative to pull-down said source terminal to about ground potential in response to voltage transitions on both an EQ line and a /WLEN line to digital "1."

10. The electrical circuit of claim 4 wherein said at least one transistor comprises two transistors operative to pull-down said source terminal to about ground potential in response to voltage transitions on both a /PSA line and a /WLEN line to digital "1."

11. The electrical circuit of claim 4 wherein said switch comprises at least one transistor operative to raise said source terminal to said voltage greater than said ground potential in response to receiving a voltage transition on a control line indicating the end of DRAM standby mode.

12. The electrical circuit of claim 11 wherein said voltage transition comprises a transition to digital "0."

13. The electrical circuit of claim 4 wherein said switch comprises at least one transistor operative to raise said source terminal to said voltage

greater than said ground potential in response to a voltage transition on a /WLEN line to digital "0."

14. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor and an n-type metal oxide semiconductor (NMOS) field-effect transistor, said circuit comprising:

first circuitry operative to maintain a source terminal of said PMOS transistor at ground potential during DRAM standby mode;

second circuitry operative to raise said source terminal to an intermediate voltage in response to a transition from said DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

third circuitry operative to raise said source terminal to a full supply voltage after said differential voltage develops between said gate terminal and said drain terminal, wherein:

said intermediate voltage is about one-half of said full supply voltage.

15. The electrical circuit of claim 14 wherein said third circuitry comprises at least one

transistor operative to raise said source terminal to said full supply voltage in response to a voltage transition on a /PSA line to digital "0."

16. The electrical circuit of claim 14 wherein said third circuitry causes said DRAM sense amplifier to be fully activated.

17. The electrical circuit of claim 14 wherein said third circuitry causes said DRAM sense amplifier to amplify said differential voltage to a full digital logic separation.

18. The electrical circuit of claim 14 further comprising fourth circuitry operative to:

pull-down a source terminal of said NMOS transistor to about ground potential after said differential voltage develops between said gate terminal and said drain terminal of said PMOS transistor and during said one of said DRAM read mode, said DRAM write mode, and said DRAM refresh mode; and

raise said source terminal of said NMOS transistor to said intermediate voltage in response to a transition from said one of said DRAM read mode, said DRAM write mode, and said DRAM refresh mode to said DRAM standby mode.

19. The electrical circuit of claim 18 wherein said fourth circuitry comprises two transistors operative to pull-down said source terminal of said NMOS transistor to said ground potential in response to a voltage transition on an NSA line to digital "1" and

to raise said source terminal of said NMOS transistor to said intermediate voltage in response to a voltage transition on said NSA line to digital "0."

20. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

a first switch operative to raise a source terminal of said PMOS transistor to a first voltage in response to a signal indicating the end of DRAM standby mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

a second switch operative to raise said source terminal of said PMOS transistor to a second voltage after said differential voltage develops, wherein:

said first voltage is less than said second voltage.

21. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type

metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

circuitry operative to maintain a source terminal of said PMOS transistor at ground potential during DRAM standby mode;

circuitry operative to raise said source terminal to an intermediate voltage in response to a voltage transition on a /WLEN line to digital "0" and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

circuitry operative to raise said source terminal of said PMOS transistor to a full supply voltage after said differential voltage develops, wherein:

said intermediate voltage is about one-half of said full supply voltage.

22. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

circuitry operative to maintain a source terminal of said PMOS transistor at ground potential prior to a voltage transition on an EQ line to digital "0;"

circuitry operative to raise said source terminal to an intermediate voltage in response to said

voltage transition on said EQ line to said digital "0" and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

circuitry operative to raise said source terminal of said PMOS transistor to a full supply voltage after said differential voltage develops and in response to a voltage transition on a PSA line to digital "0," wherein:

said intermediate voltage is about one-half of said full supply voltage.

23. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

circuitry operative to maintain a source terminal of said PMOS transistor at ground potential prior to a voltage transition on an EQ line to digital "0;"

circuitry operative to raise said source terminal to an intermediate voltage in response to a voltage transition on a /WLEN line to digital "0" and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

circuitry operative to raise said source terminal of said PMOS transistor to a full supply

voltage after said differential voltage develops and in response to a voltage transition on a /PSA line to digital "0," wherein:

said intermediate voltage is about one-half of said full supply voltage.

24. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor and an n-type metal oxide semiconductor (NMOS) field-effect transistor, said circuit comprising:

a PMOS transistor having a source terminal, a gate terminal, and a drain terminal, said source terminal of said PMOS transistor maintained at a voltage greater than ground potential, said gate terminal of said PMOS transistor operative to receive a control signal, and said drain terminal of said PMOS transistor coupled to a source terminal of said CMOS inverter PMOS transistor, wherein:

said PMOS transistor is operative to raise said source terminal of said CMOS inverter PMOS transistor to said voltage greater than ground potential in response to receiving said control signal having a voltage transition from one digital state to the other and prior to development of a differential voltage between a gate terminal and a drain terminal of said CMOS inverter PMOS transistor.

25. The electrical circuit of claim 24 wherein said drain terminal of said PMOS transistor is coupled to said source terminal of said CMOS inverter PMOS transistor via a third transistor.

26. The electrical circuit of claim 25 wherein said third transistor is a third PMOS transistor having a source terminal, a gate terminal, and a drain terminal, said source terminal of said third PMOS transistor coupled to said drain terminal of said PMOS transistor, said gate terminal of said third PMOS transistor coupled to an NSA line, and said drain terminal of said third PMOS transistor coupled to said source terminal of said CMOS inverter PMOS transistor, a voltage of said NSA line at digital "0" when said source terminal of said CMOS inverter PMOS transistor is raised to said voltage greater than ground potential.

27. The electrical circuit of claim 25 wherein said third transistor is a third NMOS transistor having a drain terminal, a gate terminal, and a source terminal, said drain terminal of said third NMOS transistor coupled to said drain terminal of said PMOS transistor, said gate terminal of said third NMOS transistor coupled to a /PSA line, and said source terminal of said third NMOS transistor coupled to said source terminal of said CMOS inverter PMOS transistor, a voltage of said /PSA line at digital "1" when said source terminal of said CMOS inverter PMOS transistor is raised to said voltage greater than ground potential.

28. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor and an n-type metal oxide semiconductor (NMOS) field-effect transistor, said circuit comprising:

a PMOS transistor having a source terminal, a gate terminal, and a drain terminal, said source terminal of said PMOS transistor maintained at a voltage greater than ground potential, said gate terminal of said PMOS transistor coupled to a /WLEN line, and said drain terminal of said PMOS transistor coupled to a source terminal of said CMOS inverter PMOS transistor, wherein:

said PMOS transistor is operative to raise said source terminal of said CMOS inverter PMOS transistor to said voltage greater than ground potential in response to a voltage transition on said /WLEN line to digital "0" and prior to development of a differential voltage between a gate terminal and a drain terminal of said CMOS inverter PMOS transistor.

29. The electrical circuit of claim 28 wherein said drain terminal of said PMOS transistor is coupled to said source terminal of said CMOS inverter PMOS transistor via an "ON" transistor.

30. The electrical circuit of claim 29 wherein said "ON" transistor is an "ON" PMOS transistor having a source terminal, a gate terminal, and a drain terminal, said source terminal of said "ON" PMOS transistor coupled to said drain terminal of said PMOS transistor, said gate terminal of said "ON" PMOS transistor coupled to an NSA line, and said drain terminal of said "ON" PMOS transistor coupled to said source terminal of said CMOS inverter PMOS transistor, a voltage of said NSA line at digital "0" when said source terminal of said CMOS inverter PMOS transistor is raised to said voltage greater than ground potential.

31. The electrical circuit of claim 29 wherein said "ON" transistor is an "ON" NMOS transistor having a drain terminal, a gate terminal, and a source terminal, said drain terminal of said "ON" NMOS transistor coupled to said drain terminal of said PMOS transistor, said gate terminal of said "ON" NMOS transistor coupled to a /PSA line, and said source terminal of said "ON" NMOS transistor coupled to said source terminal of said CMOS inverter PMOS transistor, a voltage of said /PSA line at digital "1" when said source terminal of said CMOS inverter PMOS transistor is raised to said voltage greater than ground potential.

32. A method of driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS)

inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said method comprising:

maintaining a source terminal of said PMOS transistor at about ground potential during DRAM standby mode; and

raising the voltage at said source terminal to a voltage greater than said ground potential in response to a transition from said DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor.

33. The method of claim 32 wherein said PMOS transistor comprises a low threshold voltage (V_{tp}) PMOS transistor.

34. The method of claim 33 wherein said V_{tp} is slightly greater than said differential voltage.

35. The method of claim 34 wherein said differential voltage causes said low V_{tp} PMOS transistor to turn "sub-threshold ON."

36. The method of claim 32 wherein said maintaining comprises:

receiving a voltage transition on a control line indicating DRAM standby mode; and

pulling-down the voltage at said source terminal to about ground potential in response to said voltage transition.

37. The method of claim 32 wherein said maintaining comprises pulling-down the voltage at said source terminal to about ground potential in response to voltage transitions on both an EQ line and a /WLEN line to digital "1."

38. The method of claim 32 wherein said maintaining comprises pulling-down the voltage at said source terminal to said ground potential in response to voltage transitions on both a /PSA line and a /WLEN line to digital "1."

39. The method of claim 32 wherein said raising comprises raising the voltage at said source terminal to said voltage greater than said ground potential in response to a voltage transition on an EQ line to digital "0."

40. The method of claim 32 wherein said raising comprises raising the voltage at said source terminal to said voltage greater than said ground potential in response to a voltage transition on a /WLEN line to digital "0."

41. A method of driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor and an n-type metal

oxide semiconductor (NMOS) field-effect transistor, said method comprising:

maintaining a source terminal of said PMOS transistor at about ground potential during DRAM standby mode;

raising said source terminal to an intermediate supply voltage in response to a transition from said DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

raising said source terminal to a full supply voltage after said differential voltage develops, wherein:

said intermediate supply voltage is between said full supply voltage and ground potential.

42. The method of claim 41 wherein said raising said source terminal to said full supply voltage comprises raising said source terminal to said full supply voltage in response to a voltage transition on said /PSA line to digital "0."

43. The method of claim 41 wherein said raising said source terminal to said full supply voltage causes said sense amplifier to be fully activated.

44. The method of claim 41 wherein said raising said voltage of said source terminal to said full supply voltage causes said sense amplifier to

amplify said differential voltage to a full digital logic separation.

45. The method of claim 41 further comprising:

pulling-down a source terminal of said NMOS transistor to about ground potential after said differential voltage develops between said gate terminal and said drain terminal of said PMOS transistor and during said one of said DRAM read mode, said DRAM write mode, and said DRAM refresh mode; and

raising said source terminal of said NMOS transistor to said intermediate voltage in response to a transition from said one of said DRAM read mode, said DRAM write mode, and said DRAM refresh mode to said DRAM standby mode.

46. The method of claim 45 wherein said pulling-down comprises pulling-down said source terminal of said NMOS transistor to said ground potential in response to a voltage transition on an NSA line to digital "1."

47. The method of claim 45 wherein said raising said source terminal of said NMOS transistor to said intermediate voltage comprises raising said source terminal of said NMOS transistor to said intermediate voltage in response to an NSA line transition to digital "0."

48. A method of driving a dynamic random access memory (DRAM) sense amplifier, said sense

amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said method comprising:

raising the voltage of a said source terminal of said PMOS transistor to an intermediate voltage in response to a voltage transition on a control line indicating the end of DRAM standby mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

raising said source terminal to a full supply voltage after said differential voltage develops, wherein:

said intermediate voltage is less than said full supply voltage and greater than ground potential.

49. A method of driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said method comprising:

maintaining a source terminal of said PMOS transistor at ground potential during DRAM standby mode;

raising the voltage of said source terminal to a first voltage in response to a voltage transition on a /WLEN line and prior to development of

a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

raising the voltage of said source terminal of said PMOS transistor to a second voltage after said differential voltage develops, wherein said first voltage is less than said second voltage.

50. A method of driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said method comprising:

raising the voltage of a source terminal of said PMOS transistor to a first voltage in response to a voltage transition on an EQ line and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

raising the voltage of said source terminal of said PMOS transistor to a second voltage after said differential voltage develops and in response to a voltage transition on a PSA line, wherein:

said first voltage is less than said second voltage.

51. A method of driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS)

inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said method comprising:

raising the voltage of a source terminal of said PMOS transistor to a first voltage in response to said DRAM leaving standby mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

raising the voltage of said source terminal of said PMOS transistor from said first voltage to a second voltage after said differential voltage develops.

52. A dynamic random access memory (DRAM) circuit comprising:

a complimentary pair of digital lines including a first digital line and a second digital line;

a DRAM cell operative to store a digital data bit, said DRAM cell connected to said first digital line of said complimentary pair of digital lines;

equalization and pre-charge circuitry operative to equalize and pre-charge said complimentary pair of digital lines to an intermediate voltage;

a word line operative to select said DRAM cell to cause a differential voltage to develop between said pair of complimentary pair of digital lines;

a sense amplifier operative to amplify said differential voltage to a full digital logic

separation, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said PMOS transistor having a drain terminal coupled to said first digital line and a gate terminal coupled to said second digital line; and

sense amplifier driver circuitry operative to:

maintain a source terminal of said PMOS transistor at ground potential while said equalization and pre-charge circuitry equalizes and pre-charges said complimentary pair of digital lines;

raise said source terminal to said intermediate voltage after said equalization and pre-charge circuitry ceases to equalize and pre-charge said complimentary pair of digital lines and prior to said word line causing said differential voltage to develop; and

raise said source terminal to a full supply voltage after said differential voltage develops, said intermediate voltage about one-half of said full supply voltage.

53. The DRAM circuit of claim 53 wherein said word line selects said DRAM cell for one of a DRAM read, DRAM write, and DRAM refresh operation.

54. The DRAM circuit of claim 53 wherein said source terminal raised to said full supply voltage causes said sense amplifier to amplify said

differential voltage to said full digital logic separation.

55. A system comprising:

a processor;

a memory controller;

an input/output device;

a dynamic random access memory chip comprising an array of memory cells, sense amplifier circuitry, and sense amplifier driver circuitry, said sense amplifier circuitry including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said sense amplifier driver circuitry operative to raise a source terminal of said PMOS transistor to a voltage greater than ground potential in response to a transition from DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor; and

data and control signal busing coupled to said processor, to said memory controller, to said dynamic random access memory chip, and to said input/output device.

56. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide

semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

means for switching a source terminal of said PMOS transistor to a voltage greater than ground potential in response to a transition from DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor.

57. An electrical circuit for driving a dynamic random access memory (DRAM) sense amplifier, said sense amplifier including a latch formed by cross-coupling a first complimentary metal oxide semiconductor (CMOS) inverter and a second CMOS inverter, said first CMOS inverter having a p-type metal oxide semiconductor (PMOS) field-effect transistor, said circuit comprising:

means for maintaining a source terminal of said PMOS transistor at about ground potential during DRAM standby mode; and

means for raising the voltage at said source terminal to a voltage greater than said ground potential in response to a transition from said DRAM standby mode to one of DRAM read mode, DRAM write mode, and DRAM refresh mode and prior to development of a differential voltage between a gate terminal and a drain terminal of said PMOS transistor.